REMARKS

Claims 1-30 are pending in the present application. Claims 1 and 2 have been combined herein. In view of the below comments it is respectfully submitted that each of these claims is allowable.

Applicant wishes to thank the examiner for allowing claim 6 and indicating the allowable subject matter of claims 2-8 and 10-14.

Claims 1, 9 and 15-30 have been rejected under 35 USC §102(b) as being anticipated by Takahashi, et al. (5,748,024). Applicant respectfully traverses this rejection.

Claim 2 has been amended to be placed in independent form. Claim 1 has also been cancelled. In view of the examiners indication of allowability, it is respectfully submitted that claims 2-8 are in condition for allowance.

Claim 9 specifically recites, "an input note to receive and input signal, the input signal varying between a first voltage level and a second voltage level." The claim further requires "a second p-channel transistor having a first source/drain region coupled to the second source/drain of the fist p-channel transistor, a second source/drain region coupled to a third reference node and a gate coupled to a second enable signal node, the third reference node carrying a third voltage level, the third voltage level being different than the first voltage level." It is respectfully submitted that the Takahashi reference does not teach or suggest the limitations of claim 9.

In making the rejection, the Examiner pointed to Takahashi's Figure 4 and stated that input node 31 receives an input signal varying between a first voltage level and a second voltage level and p-channel transistor 21 has a second source/drain coupled to a third voltage node. It is respectfully submitted that this reading of the prior art is inconsistent with the references teachings. In fact, the reference does not anticipate the claim.

Takahashi teaches that the input signal 31 of Figure 4 varies between ground and the voltage level VDD, which is also provided to transistor 21. This can be seen by referring to Figure 1a and Figure 4, along with the associated portions of the specification. In particular, the Takahashi reference specifically recites:

> A signal outputted from a circuit located on a preceding portion is inputted to the level shift circuit 100 to convert the signal to a predetermined level, which corresponds to an operational voltage level of the buffer circuit 200, and an output signal of the level shift circuit 100 is led to the buffer circuit 200. [Col. 4, lines 25-30]

From this paragraph it is clear that the output of level shift circuit 100 provides the input of buffer circuits 200 and that input signal "corresponds to an operational voltage level of the buffer circuit 200." The specification also makes it clear that the circuit of Figure 4 is the output buffer 200. "FIG. 2 is a diagram illustrating a first embodiment of the buffer circuit in the level convertor according to the present invention." Col. 4, lines 57-59. "FIG. 4 is a diagram illustrating a second embodiment of the FIG. 2." Col. 3, lines 59-60. *See also* col. 5, lines 30-31 ("FIG. 4 shows a buffer circuit according to a second embodiment of the present invention"). It is respectfully submitted that claim 9 is allowable over the references of record.

Claims 10-19 depend from claim 9 and add further limitations. It is respectfully submitted that each of these claims is allowable for reason of depending from an allowable claim as well for adding further limitation.

Claim 20 specifically recites, "an enable/disable section including a first portion coupled between the level shifting section and the first voltage node and a second portion coupled between the level shifting section and third reference voltage node." It is respectfully submitted that the reference of record does not teach or suggest the limitations of claim 20.

In making the rejection, the examiner once again pointed to Figure 4 of the Takahashi

reference. In this rejection the examiner referred to transistors 22 and 23 as being portions of the level shifting circuit. As discussed above, however, these two transistors are not part of the level shift circuit 100 but rather a part of the output buffer 200. This fact is clearly disclosed in the Takahashi reference. See col. 5, lines 30-33. As a result, the Takahashi reference does not teach or suggest an enable/disable section including a first portion coupled between the level shifting section and the first reference voltage node and a second portion coupled between the level shifting section and a third reference voltage node.

Since the Takahashi reference does not teach or suggest the limitations of claim 20, it is respectfully submitted that this claim is allowable.

Claims 21-30 depend from claim 20 and add further limitations. It is respectfully submitted that each of these claims is allowable for reason of depending from an allowable claim as well for adding further limitation.

In view of the above, Applicants respectfully submit that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicants request that the Examiner contact Applicants' attorney at the address below.

Respectfully submitted,

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Date

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